International Journal on Emerging Technologies 11(3): 701-706(2020)

ISSN No. (Print): 0975-8364
ISSN No. (Online): 2249-3255

NPC-VSI Operated PLL Based SSSC for Transmission Line Power Flow Control

Shaik Rafi Kiran[1], J.T. Ramalingeswar[2] and S. Varadarajan[3]

[1]Professor & HOD, Department of Electrical and Electronics Engineering, SVEC, Tirupati, (Andhra Pradesh), India.
[2]Research Scholar, Department of Electrical Engineering, VIT University, Vellore (Tamilnadu), India.
[3]Professor, Department of Electronics and Communication Engineering, S V University (Andhra Pradesh), India.

(Corresponding author: Shaik Rafi Kiran)

(Received 01 April 2020, Revised 07 May 2020, Accepted 09 May 2020)
(Published by Research Trend, Website: www.researchtrend.net)

ABSTRACT: Due to the sudden changes of loads in distribution network, the voltage and frequency of the power system get unbalanced. In order to overcome this drawback, in this article the Discrete Direct Controller (DDC) and Discrete Indirect Controller (DIC) with Phase Locked Loop (PLL) based Static Synchronous Series Compensator (SSSC) is proposed to control the transmission line voltage. The three level Neutral Point Clamped (NPC) Voltage Source Inverter (VSI) is used to convert DC to AC. DDC and DIC's generate switching pulses for 3-level VSI by the use of PLL. Here, the three phase voltage components (a, b, c) are converted to (α, β, 0) by using PLL instead of reference wave generator. The PLL is used to compare source side voltage with receiver side voltage. Based on the resultant signal, a step change in transmission line reactance occurs. Moreover, the PLL is used to improve the dynamic performance of transmission system. The results of SSSC are verified by using MATLAB/Slink software.

Keywords: DDC, DIC, NPC-VSI, PLL, SSSC.

I. INTRODUCTION

According to the latest surveys, there is a significant rise in the electricity usage due to the increased population and usage of electrical appliances for domestic as well as industrial applications. Hence, it is necessary to use the power generation and transmission effectively [1]. At present, the major problem in interconnected power transmission systems is controlling of financial constraints, stability limits and load disturbances. When the loads are interconnected, frequency disturbances create a severe problem in power system. To overcome this problem, conventional governor control technique is used, but it gives a slow transient response. So, dynamic performance of SSSC is used to compensate the frequency of oscillations and load disturbances [2].

A SSSC is a Flexible Alternating Current Transmission System (FACT'S). Basically, FACT'S operation is involved with power electronic devices. FACT'S Controller is classified into two types, one is conventional type and another one is non-conventional type. Conventional FACT'S controller consists of resistor, capacitor and inductor. Non-conventional FACT'S devices consist of thyristors and Gate Turn-Off (GTO) devices. Thyristor control-based FACT'S devices are static condenser, static-var compensator and series-controlled compensator. GTO, Insulated Gate Bipolar Transistor (IGBT) control-based FACT'S devices are static compensator, SSSC and unified power flow controllers. SSSC is a solid-state voltage source device which gives a controllable AC source. This SSSC is connected in series with the transmission line through a coupling transformer. SSSC controls the transmission line voltage effectively and efficiently [3].

In electrical power system, the power flow control has been done by controlling the voltage magnitude and phase angle of the transmission system with DDC and DIC. In SSSC, 3-level NPC-VSC is used to convert the fixed DC to variable AC [4]. The difference between SSSC and Static Synchronous Compensator (STATCOM) is that SSSC is connected in series with the electric power system, whereas STATCOM is connected in parallel with the transmission system. The main contribution in this paper is the design of DDC and DIC by the use of PLL, generating switching pulses for NPC-VSI and by using dynamic response of SSSC frequency of oscillations and load disturbances are compensated.

II. STATIC SYNCHRONOUS SERIES COMPENSATOR

A. Operation of SSSC

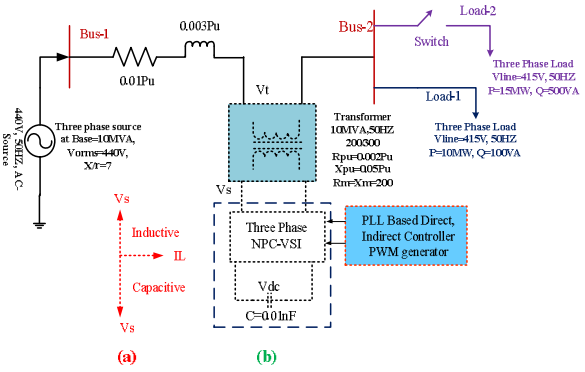


Fig. 1. SSSC Phasor diagram, (b) SSSC based interconnected electrical power system.

The main function of PLL is used in SSSC is to reduce inherent time delay. As a result, dynamic performance of SSSC is improved. SSSC has two modes of operation, inductive and capacitive. In inductive mode, SSSC injected voltage is leading the transmission line current and in capacitive mode injected voltage is lagging the transmission line current.

The block diagram of SSSC is shown in Fig. 1. And the corresponding phasor diagram is shown in Fig. 2, [5, 6]. In SSSC, source voltage (Vs) lags the transmission line terminal voltage (Vt). Hence, the real power flows from transmission line to the dc capacitor through a NPC-VSI. If Vs leads Vt and real power flows from SSSC to the transmission line through a coupling transformer [10, 12].

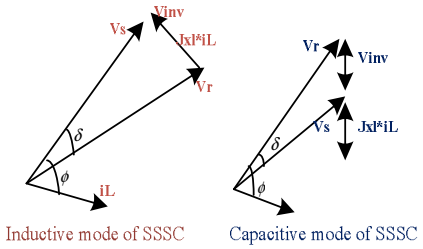


Fig. 2. Phasor diagrams of SSSC.

Control structure of PLL consists of reactance controller, phase angle and inverter gate pattern logic controller. The reactance controller finds change in transmission line reactance and summing with reference reactance. Based on resultant signal of reactance, the transmission line voltage or current transient and steady state response is improved. The PLL block is used to control the phase angle between the source voltage and transmission line current by giving PWM pulses to the NPC-VSI.

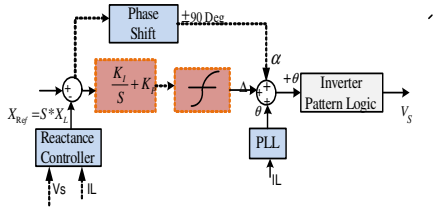


Fig. 3. Basic control structure of PLL.

The Insulated Gate Bipolar Transistor (IGBT) is used to design a NPC-VSI because of its high switching frequency, less power dissipation and high input impedance. Moreover, IGBT's are used to operate at high voltage rating applications and it is having high temperature withstand capability. The unbalance in the neutral point of the dc-link capacitors is overcome by using zero sequence components. Based on series reactance compensation, the control scheme of SSSC is shown in Fig. 3 [11]. The block diagram of NPC-VSI is shown in Fig. 4. The IGBT's parallel diodes are useful to protect switches from overvoltage's.

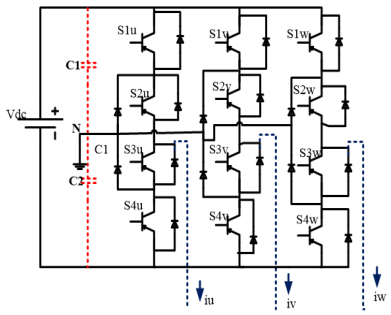


Fig. 4. Schematic of NPC-VSI.

B. Neutral point clamped voltage source inverter

The NPC-VSI input dc-link capacitors are used to store the electrical energy. A N-Level NPC-VSC is designed with N-1 input dc capacitors, 2(N-1) per phase IGBT switches and 2 (N-2) antiparallel bypass diodes. The inverter inputs dc voltage is converted into three level stepped voltages by the used of dc-link capacitors C_1 and C_2 and each capacitor charging up to $V_{dc}/2$.

NPC-VSI is used for high power applications and it gives a good performance for DC to AC conversion. Moreover, this inverter gives low total harmonic distortion and it works up to a switching frequency of 500Hz. The operation of switches in NPC-VSI is shown in Table 1. To achieve high levels of output voltage by adding additional power semiconductor devices in NPC-VSI. As a result, there is a less harmonic ripple in the output voltage.

The main difference between two- level and three level inverters is clamping diodes. For the conversion of DC-bus voltage to three level voltage ($V_{dc}/2$, 0, $-V_{dc}/2$) diode D_1 and D_4 are used is shown in Fig. 4. Unlike two level converters, the three level converters are capable of controlling the output voltage magnitude by controller input dc voltage. The dc capacitor voltage control is obtained by displacement, Δα, between the SSSC and transmission line voltage. In this, the three-phase system (a, b, c) is converted to (α, β, 0) system by using matrix quotations (3), (4), (5) [6, 11].

By the series connection of input capacitor, many researchers have developed different types of multilevel VSI's for high power applications, but the main drawback is unbalance in input capacitors. However, in case of NPC-VSI, balance of input capacitors easily maintained by the use of zero sequence component and without usage of additional transformer and reactance, the three levels neutral point clamped voltage source inverter generates five levels VSI [7]. The switching pulses generated by the use of PWM technique for NPC-VSI is shown in Fig. 5.

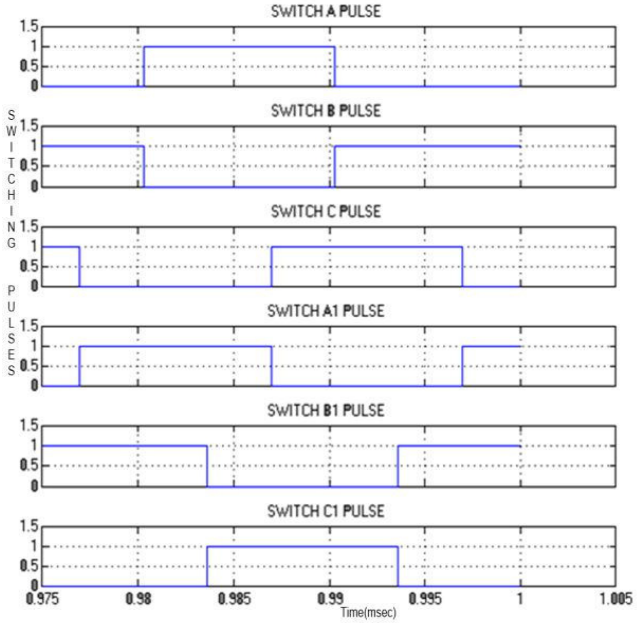


Fig. 5. Switching pulses for NPC-VSC.

Table 1: Switching scheme of NPC-VSI.

Device	V_x=+E	V_x=N	V_x=-E
S_{1u}	On	Off	Off
S_{2u}	On	On	Off
S_{3u}	Off	On	On
S_{4u}	Off	Off	On
Q_x	+	N	-

where,
V_x= Phase to neutral voltage
Q_x= Switch operation
x= u, v, w
Due to the average current flow in or out of the neutral point, the neutral point of NPC-VSI varies. As a result, the imbalance occurs in switches. Hence, the neutral point varies from center point of the input dc-link. However, the main problem in NPC-VSI is over voltage that appears on the switches. [8].

III. PLL Based Discrete Direct Controller

A. Design of DDC
The PLL based DDC is used to control voltage magnitude and phase angle of transmission line voltage by the displacement of input dc capacitor voltage kept constant in DDC [9]. The SSSC generates three phase voltages from an input DC capacitor and it is connected in series with the transmission line through a coupling transformer. The injected voltage is in phase quadrature with the transmission line current.
The schematic of simulated PLL based DDC is shown in Fig. 6. From Fig. 6, in operation of DDC, initially the reference voltage V_{ref} is compared with SSSC input dc capacitor voltage and the error signal is given to PI controller-1. PI controller-1 signal is summed with phase "a" positive sequence component and the resultant signals are given to PWM generator. After that SSSC injected voltage is given to PLL-1, which consists of automatic voltage gain controller. Based on the input signal given to the PLL-1, it synchronizes input sinusoidal signals, phase error and variable frequency of transmission line voltage and current.
PLL-1 gives the zero-sequence sinusoidal signal of phase "a" to the transformation block of (abc/dq0). As a result, d, q, 0 components are generated and finally a, b, c signals are given to PWM generator. Based on source, load and transmission line voltage, DDC generates PWM pulses. Based on PWM pulses, NPC-VSI generates three phase transmission compensated voltage.

B. Dynamic performance of SSSC with DDC
Performance of PLL based DDC and how it affects the operation of SSSC with electrical system, using NPC-VSI is shown in Fig.6. The DDC operation depends on d-q transformation with the help of this d-q transformation, it is possible to control the reactive power in between the transmission line and SSSC [10]. In general, PLL gives synchronizing signal and phase angle of the transmission system. When SSSC operates in direct control mode, the PI controller parameters are considered as, Kp = 0.5 and Ki = 0.35. Two level converters do not have voltage control capability, but they control the phase angle by the use of gate signals. The step change in transmission line reactance is shown in Fig. 7.

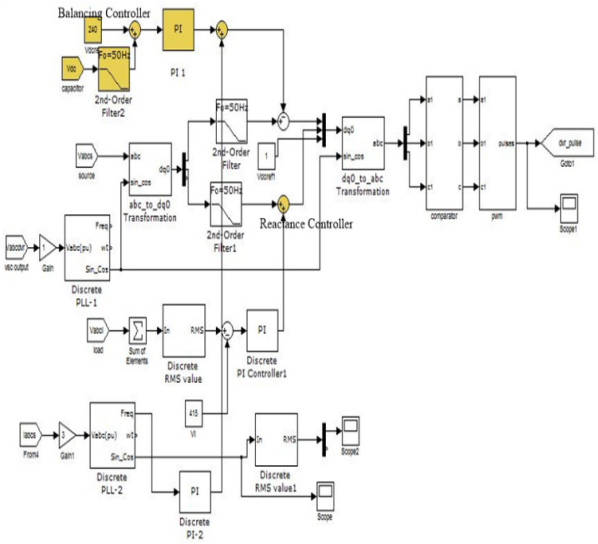


Fig. 6. PLL based DDC PWM generator.

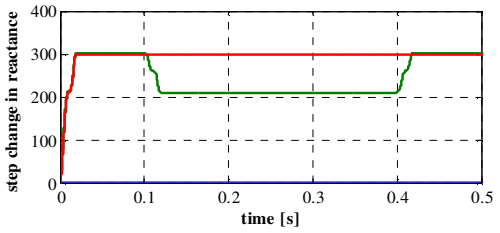


Fig. 7. Step change in transmission line reactance.

IV. PLL BASED DISCRETE INDIRECT CONTROLLER

A. Design of DIC
The main theme of SSSC is to control transmission line active and reactive power this can be controlled by the help of DIC. In DIC, transmission line reactance is compensated by injecting the series compensation reactance Xs, or, by injecting the series compensation voltage source Vs. In some practical situations reactance control is the most preferred in DIC and it is shown in Fig. 8.

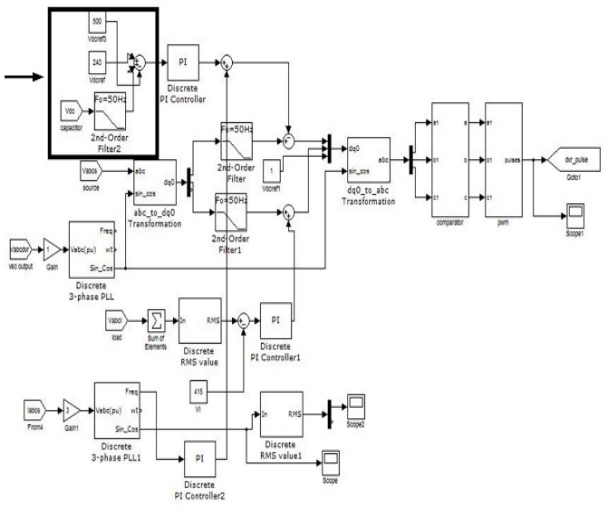


Fig. 8. PLL based DIC PWM generator.

The value of series compensation, S is calculated as the ratio of injected reactance (Xs) to the transmission line reactance (Xt) [11]. If injected or reference reactance is positive, the SSSC acts as capacitive compensation mode, if it is negative SSSC acts as inductive compensation. To get the reference reactance and zero sequence component, the three-phase voltage system a, b, c is converted into stationary reference frame α, β, 0 and its equivalent indirect control is shown in Fig. 9 [3].

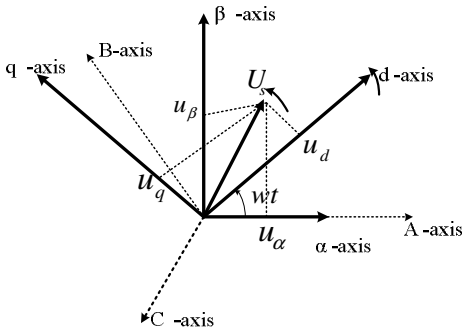


Fig. 9. Three phase components transformation phasor diagram.

Degree of series compensation is derived as,

$$S = \frac{X_S}{X_t} \quad (1)$$

Injected series reactance is calculated as,

$$X_S = S \times X_t \quad (2)$$

$$\begin{bmatrix} V_{inj-\alpha} \\ V_{inj-\beta} \\ V_{inj-0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} V_{inj-a} \\ V_{inj-b} \\ V_{inj-c} \end{bmatrix} \quad (3)$$

In DDC the conversion of all the factors is same as DIC, but the difference is VSI input side voltage variation. The current conversion of α, β, 0 to a, b, c is follows as,

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (4)$$

The conversion of d, q, 0 to α, β, 0 equations are as followed in Eqn. 5,

$$\begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} = \begin{bmatrix} \frac{i_\alpha}{i_{\alpha\beta}} & \frac{i_\beta}{i_{\alpha\beta}} & 0 \\ -\frac{i_\beta}{i_{\alpha\beta}} & \frac{i_\alpha}{i_{\alpha\beta}} & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \quad (5)$$

Where, $i_{\alpha\beta} = \sqrt{i_\alpha^2 + i_\beta^2}$

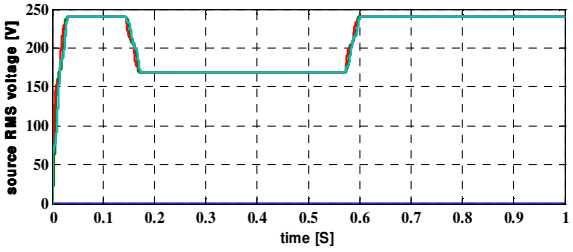
By using Eqns. (3), (4) and (5) equations, three phase voltage system a, b, c is converted to α, β, 0 components and the corresponding phasor diagram is shown in below Fig. 9.

B. Dynamic performance of SSSC with DIC

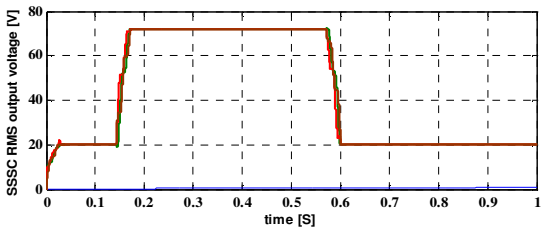
Performance of PLL based DIC and how it affects the operation of SSSC with electrical system, using NPC-VSC is shown in Fig. 8. Design and operation DIC is same as DDC. Here, the PLL of DDC, conversion of three phase components, balancing of neutral point of NPC-VSI and the values of proportional and integral (PI) controller are the same as DIC. DIC transmission line voltage constant with respect to load, but the phase angle of the transmission line is compensated by using DIC.

V. SIMULATION RESULTS

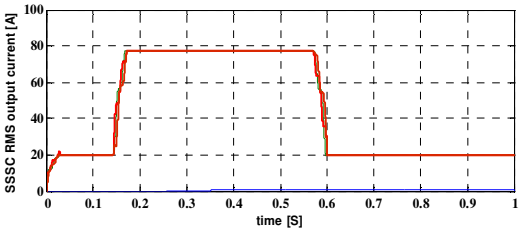
From the output wave forms of Fig. 10, it is clearly observed that, load one is operated up to 0.4ms. After 0.4ms, load two is added as additional to load one. As a result, the transmission line voltage drops from the instant of 0.4ms to 0.7ms. The transmission voltage drop is compensated by the use of PLL based DDC SSSC. Due to sudden change in load, the fluctuations occurred at point 0.4ms and 0.7ms of output waveform and harmonic distortion, which can be compensated by the use of PLL. When SSSC operates in DIC mode, the simulated wave forms of SSSC injected, dc capacitor voltage and source, load voltage and load current is shown in Fig. 11, and the DDC and DIC operating parameters is shown in Table 2.



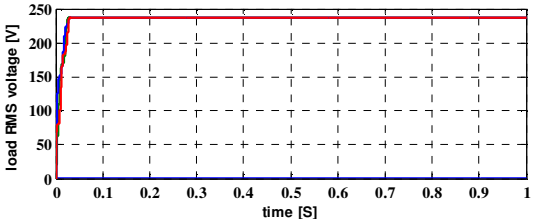
(a)



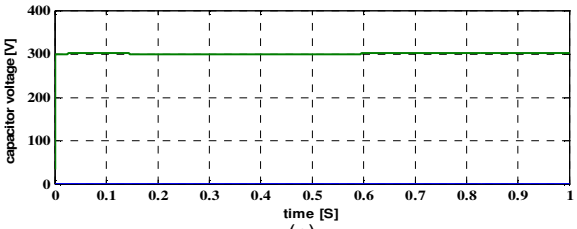
(b)



(c)

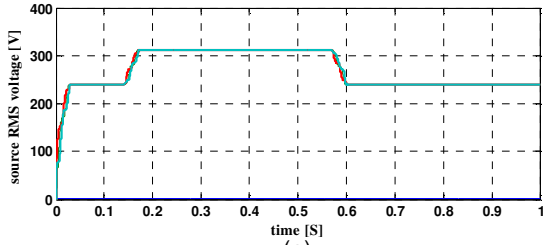


(d)

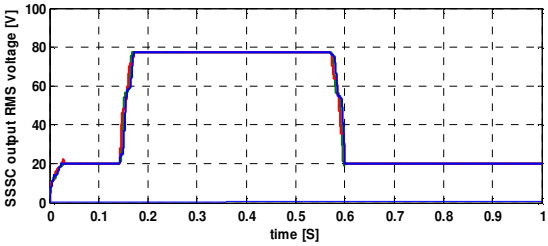


(e)

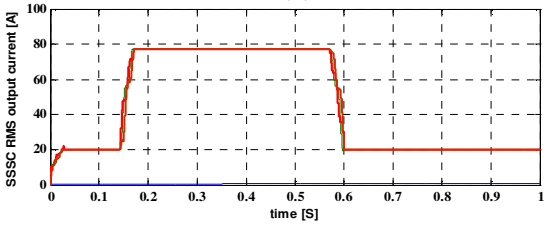
Fig. 10. Simulation results of DDC based SSSC, (a) Source voltage, (b). SSSC output voltage, (c) SSSC output current, (d) Load voltage and (e) Voltage across DC-link capacitor.



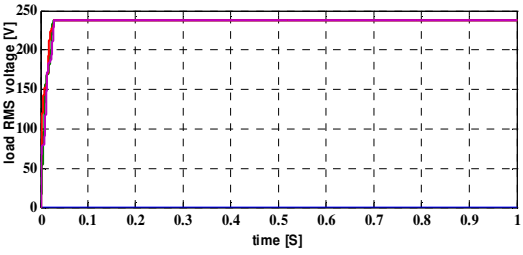
(a)



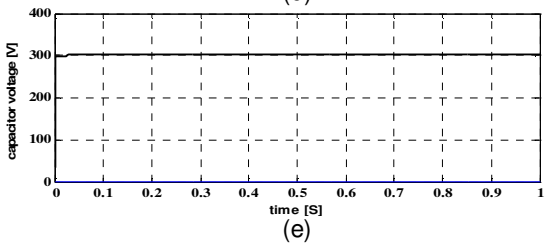
(b)



(c)



(d)



(e)

Fig. 11. Simulation results of indirect controller, (a) Source voltage, (b) SSSC output voltage, (c) SSSC output current, (d) Load voltage and (e) Voltage across DC-link capacitor.

Table 2: Performance parameters of DDC and DIC when step change in rectance.

Parameters	Values
DDC (30% step change in X_L)	
Injected Reactance	30.6 %
SSSC Apparent power	5.18 kVA
Source Voltage	240 V
Step up Transformer	200/300 V
SSSC Injected Voltage	72 V
SSSC Injected Current	72 A
Load Voltage	240 V
Line reactance	3 mH
Line resistance	0.01 Ω/Phase
DC-Side Voltage	300 V
DIC (30% step change in X_L)	
Injected Reactance	30.6 %
SSSC Apparent power	5.184 kVA
Source Voltage	240 V
Step up Transformer	200/300 V
Injected Voltage	72 V
Injected Current	72 A
Load Voltage	240 V
Line reactance	3 mH
Line resistance	0.01 Ω/Phase
DC-Side Voltage	300-310 V

VI. CONCLUSION

Instead of reference wave generator the DDC and DIC are designed by the use of PLL. The PLL based DDC and DIC are generated switching pulses for NPC-VSI. Due to this switching scheme, the fluctuations in the injected transmission line voltage and current are reduced and there by steady state response is improved. Due to less harmonic content, NPC-VSC is used instead of conventional converter. From the simulated results of Fig. 7 and 11, it is observed that discrete PLL based DDC and DIC's improved the dynamic behavior of SSSC.

VII. FUTURE SCOPE

The future scope of the work is the application of DDC and DIC for static compensator and static synchronous reactance.

Conflict of Interest. No conflict of interest

REFERENCES

[1]. Vergara-Dietrich, J. D., Morato, M. M., Mendes, P. R., Cani, A. A., Normey-Rico, J. E., & Bordons, C. (2019). Advanced chance-constrained predictive control for the efficient energy management of renewable power systems. *Journal of Process Control*, *74*, 120-132.

[2]. Ain, Q., Jamil, E., Hameed, S., & Naqvi, K. H. (2020). Effects of SSSC and TCSC for enhancement of power system stability under different fault disturbances. *Australian Journal of Electrical and Electronics Engineering*, *17*(1), 56-64.

[3]. Chethan, H. R., & Mageshvaran, R. (2020). Stability Improvement Using SSSC in Synchronous Generation System with PMSG-Based Offshore Wind Farm. In *Advances in Communication, Signal Processing, VLSI, and Embedded Systems*, 535-546.

[4]. Basha, C. H., Chowdary, V. G., Rani, C., Brisilla, R. M., & Odofin, S. (2020). Design of SVPWM-Based Two-

Leg VSI for Solar PV Grid-Connected Systems. In *Soft Computing for Problem Solving*, 879-892.
[5]. Smolovik, S. V., Chudny, V. S., Denisenko, A. I., Liamov, A. S., & Tupitsina, A. L. (2020). Control Characteristics of Static Synchronous Series Compensator. In *2020 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus)*, 1329-1332.
[6]. Purohit, A., & Gohokar, V. (2019). Maloperation of Distance Relay under Faulty Conditions in presence of Static Synchronous Series Compensator. In *2019 IEEE 2nd International Conference on Power and Energy Applications (ICPEA)*, 66-70.
[7]. Basha, C. H., Rani, C., & Odofin, S. (2017). A review on non-isolated inductor coupled dc-dc converter for photovoltaic grid-connected applications. *International Journal of Renewable Energy Research (IJRER)*, *7*(4), 1570-1585.
[8]. Basha, C. H., Bhanutej, J. N., Rani, C., & Odofin, S. (2019). Design of an LPF Based Slider Controller for THD Reduction in Solar PV B-4 Inverter. In *2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT),* 1-9.
[9]. Jiang, W., Wang, W., Ma, M., Zhai, F., & Wang, J. (2019). Comments on "Improved Virtual Space Vector Modulation for Three-Level Neutral-Point-Clamped Converter with Feedback of Neutral-Point Voltage". *Transactions on Power Electronics*, *34*(4), 3996-3996.
[10]. Sreenivasan, G., & Sudarsan, K. (2020). Power Quality Enhancement in Grid Connected Hybrid PV/WT System using Tree Seed Algorithm with RNN. *Helix*, *10*(02), 211-218**.**
[11]. Sreedharan, S., Joseph, T., Joseph, S., Chandran, C. V., Vishnu, J., & Das, V. (2020). Power system loading margin enhancement by optimal STATCOM integration–A case study. *Computers & Electrical Engineering*, *81*, 106521.
[12]. Masood, A., Xin, A., Salman, S., Jan, M. U., Iqbal, S., Rehman, H. U., & Simiyu, P. (2020). Performance Analysis of FACTs Controller for Congestion Mitigation in Power System. In *2020 3rd International Conference on Computing, Mathematics and Engineering Technologies (iCoMET)*, 1-6.

How to cite this article: Kiran, S. R., Ramalingeswar, J. T. and Varadarajan, S. (2020). NPC-VSI Operated PLL Based SSSC for Transmission Line Power Flow Control. *International Journal on Emerging Technologies*, *11*(3): 701–706.